W

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,604	10/08/2003	Andrew W. Dornbusch	SILA:175	7202

7590 09/13/2006

Brian W. Peterman
O'KEEFE, EGAN & PETERMAN
Building C, Suite 200
1101 Capital of Texas Highway South
Austin, TX 78746

EXAMINER	
CHAN, RICHARD	
ART UNIT	**PAPER NUMBER**
2618	

DATE MAILED: 09/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/681,604	**Applicant(s)** DORNBUSCH, ANDREW W.
	Examiner Richard Chan	**Art Unit** 2618

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *12 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-16,18-30,32-34 and 36-39* is/are pending in the application.

4a) Of the above claim(s) *5,17,31 and 35* is/are withdrawn from consideration.

5)☒ Claim(s) 14-*16,18-26,32-34 and 36-39* is/are allowed.

6)☒ Claim(s) *1-4 and 27-30* is/are rejected.

7)☒ Claim(s) *6-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/12/06* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date *1/20/04*.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1, 2, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagen (US 6,980,116 B2) in view of Durst (US 2002/0003493).

With respect to claim 1, Hagen discloses an antenna error detection and circuit protection system, comprising: a current limit detection circuit **Fig.1** integrated within an integrated radio receiver and configured to detect current levels through **node 170** drawn by at least one antenna mounted remotely from the integrated radio receiver frp, **node 120**, the current limit detection circuit having a gate drive signal **105** as an output; and a current limiting pass transistor **110** having its source and drain coupled between a supply voltage from **node 150** and an antenna from **node 120** and having its gate **105** coupled to the gate drive signal from **I_monitor**; wherein the current limit detection circuit is configured to adjust the gate drive signal to reduce current flow through the pass transistor when the detected current level drawn by the at least one antenna rises above a current limit level **Col.1-2 lines 40-19.,** however the Hagen reference does not disclose wherein a terrestrial antenna and a satellite antenna are coupled to the current limit detection circuit and to the current limiting pass transistor.

The Durst reference however discloses wherein a satellite and terrestrial antenna are coupled together within a receiver system. Fig.4 (Paragraph 0031)

It would have been obvious to one of ordinary skill in the art to implement the antenna error detection system as disclosed by Hagen with the receiver that is capable of satellite and terrestrial communication in order to receive error free signals within the terrestrial and satellite environment.

With respect to claim 2, Hagen and Durst combined discloses the system of claim 1, however Hagen continues to disclose wherein the current limiting pass transistor **110** is an external transistor device **Col.1 lines 40-47**.

With respect to claim 27, Hagen discloses a method for detecting errors in and protecting antenna circuitry, comprising: detecting current levels drawn by at least one antenna mounted remotely from the integrated radio receiver; generating a gate drive signal **105** based upon the detected current levels through current detection **node170**; controlling current through a current limiting pass transistor **110** with the gate drive signal, the current limiting pass transistor having its source and drain coupled between a supply voltage node **150** and an antenna node **160** and having its gate coupled to the gate drive signal **105**; and adjusting the gate drive signal to reduce current flow through the pass transistor when the detected current level drawn by the at least one antenna rises above a current limit level **Col.1-2 lines 40-19**, ., however the Hagen reference does not disclose wherein a terrestrial antenna and a satellite antenna are coupled to the current limit detection circuit and to the current limiting pass transistor.

The Durst reference however discloses wherein a satellite and terrestrial antenna are coupled together within a receiver system. Fig.4 (Paragraph 0031)

It would have been obvious to one of ordinary skill in the art to implement the antenna error detection system as disclosed by Hagen with the receiver that is capable of satellite and terrestrial communication in order to receive error free signals within the terrestrial and satellite environment.

With respect to claim 28, Hagen and Durst combined discloses the method of claim 27, however Hagen continues to disclose wherein the current limiting pass transistor **110** is an external transistor device **Col.1 lines 40-47**.

3. Claims 3 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagen (US 6,980,116 B2) and Durst (US 2002/0003493) in view of Ward (US 6,928,281).

With respect to claim 3, Hagen and Durst combined disclose the system of claim 1, however both references do not disclose wherein the current limiting pass transistor is a transistor device integrated within the integrated radio receiver.

The Ward reference however discloses wherein a current limiting pass transistor **62** is within a current limiting device **43,** and the current limiting device is located within the interface module **24** of the receiver **10 in Fig.1**.

It would have been obvious to one of ordinary skill in the art to implement a transistor device integrated within the integrated radio receiver as disclosed by Ward to the receiver of Hagen in order to have one module to process the current limit process.

With respect to claim 29, Hagen and Durst combined disclose the method of claim 27, however both reference does not disclose wherein the current limiting pass transistor is a transistor device integrated within the integrated radio receiver.

The Ward reference however discloses wherein a current limiting pass transistor **62** is within a current limiting device **43,** and the current limiting device is located within the interface module **24** of the receiver **10 in Fig.1**.

It would have been obvious to one of ordinary skill in the art to implement a transistor device integrated within the integrated radio receiver as disclosed by Ward to the receiver of Hagen in order to have one module to process the current limit process.

4. Claims 4 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hagen (US 6,980,116 B2) and Durst (US 2002/0003493) in view of Stiefel (US 5,721,774).

With respect to claim 4, Hagen and Durst combined disclose the system of claim 1, however both references combined does not disclose specifically the system further comprising a voltage protection device coupled between the current limiting transistor and the at least one antenna.

The Stiefel reference however discloses a current limiting transistor **Q163** that is connected to diode **D63**, protecting the circuit from voltage issues.

It would have been obvious to one of ordinary skill in the art to implement a diode the current limiting transistor with a diode as a voltage protection circuit coupled to at least one antenna, in order to shield the transistor from any voltage spikes incoming from the antenna.

With respect to claim 30 Hagen and Durst combined disclose the method of claim 27, however both references do not disclose further comprising providing a voltage protection device coupled between the current limiting transistor and the at least one antenna.

The Stiefel reference however discloses a current limiting transistor **Q163** that is connected to diode **D63**, protecting the circuit from voltage issues.

It would have been obvious to one of ordinary skill in the art to implement a diode the current limiting transistor with a diode as a voltage protection circuit coupled to at least one antenna, in order to shield the transistor from any voltage spikes incoming from the antenna.

Allowable Subject Matter

5. Claims 6-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 14-16, 18-26, 32-34, abd 36-39 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 14, Ward discloses an antenna error detection and circuit protection system, comprising: a current **43** and voltage detection circuit **46** and **50** in interface module **24**, integrated within an integrated radio receiver **10** and configured to detect current and voltage levels drawn by at least one antenna **30** mounted remotely from the integrated radio receiver in antenna module **11**, the current and voltage detection circuit configured to determine under-current, over-current, and over-voltage antenna error conditions **Col.3 lines 32-49 and Col.4 lines 14-29**; and at least one antenna error output pin **35** for the integrated radio receiver, the antenna error output pin providing an output signal indicative of an antenna error condition **(Col. 3 lines 23-29),** however the prior art does not disclose wherein a terrestrial antenna and a satellite antenna are coupled to the current and voltage detection circuit, the current and voltage detection circuit being configured to determine under-current, over-current, and over-voltage antenna error conditions for the terrestrial antenna and the satellite antenna.

Claims 15, 16, and 18-26 are dependent on claim 14.

With respect to claim 32, Ward discloses a method for detecting errors in and protecting antenna circuitry, comprising: detecting current levels drawn by at least one antenna mounted remotely to an integrated radio receiver **10** to determine under-current, over-current, and over-voltage antenna error conditions; detecting voltage levels drawn by at least one antenna mounted remotely from the integrated radio receiver to determine under-current, over-current, and over-voltage antenna error conditions **Col.3 lines 32-49 and Col.4 lines 14-29**; and utilizing at least one antenna error output pin **35** for the integrated radio receiver to provide an output signal indicative of an antenna error condition, however the prior art does not disclose wherein a terrestrial antenna and a satellite antenna are coupled to the integrated radio receiver and wherein the detecting steps comprise detecting current and voltage levels for both the terrestrial antenna and the satellite antenna.

Claims 33, 34, and 36-39 are dependent on claim 32.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Chan whose telephone number is (571) 272-0570. The examiner can normally be reached on Mon - Fri (9AM - 5PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571)272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Chan
Art Division 2618
08/31/06

9/4/06

QUOCHIEN B. VUONG
PRIMARY EXAMINER